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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	6	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and environment and ASIC and time and table and error and node and predict\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/27 20:44
L3	1	Lin and converfication	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/27 18:01
L4	0	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and environment and ASIC and time and table and error and node and predict\$5 and I3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/27 18:14
L5	0	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and time and table and error and node and predict\$5 and I3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/27 18:14
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L11	1	HDL and (circuit same emulat\$4) and propagation and verification and environment and ASIC and time and table and error and node and predict\$5 and I3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/27 18:14
L12	979	703/23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/27 20:44
S1	3	"2002073375"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:35
S2	3	("2002073375").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/09/23 22:35
S3	8	hollander and yoav	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:40
S4	25	HDL and "C++" and (circuit same emulat\$4) and propagation and verification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:52
S5	25	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and environment	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:52

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S6	22	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and environment and ASIC	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:52
S7	22	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and environment and ASIC and time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:53
S8	22	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and environment and ASIC and time and table	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:53
S9	22	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and environment and ASIC and time and table and error and node	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:53
S10	6	HDL and "C++" and (circuit same emulat\$4) and propagation and verification and environment and ASIC and time and table and error and node and predict\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/27 18:13
S11	64	(HDL VHDL Verilog) and "C++" and (circuit same emulat\$4) and propagation and verification and environment and ASIC and time and table and error and node and predict\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/23 22:56


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Relevance scale ☐ ☐ ☐ ☐ ☐**1** [Functional verification of large ASICs](#)

Adrian Evans, Allan Silburt, Gary Vrckovnik, Thane Brown, Mario Dufresne, Geoffrey Hall, Tung Ho, Ying Liu

May 1998 **Proceedings of the 35th annual conference on Design automation****Publisher:** ACM Press

Full text available: pdf(263.28 KB)

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This paper describes the functional verification effort during a specific hardware development program that included three of the largest ASICs designed at Nortel. These devices marked a transition point in methodology as verification took front and centre on the critical path of the ASIC schedule. Both the simulation and emulation strategies are presented. The simulation methodology introduced new techniques such as ASIC sub-system level behavioural modeling, large multi-chip simulations, ...

Keywords: ASIC verification, emulation, simulation**2** [Practical concurrent ASIC and system design and verification](#)

I. Gibson, C. Amies

March 1997 **Proceedings of the 1997 European conference on Design and Test****Publisher:** IEEE Computer Society

Full text available: pdf(622.26 KB)

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This paper describes the evolution of a design and verification methodology successfully used to develop advanced ASICs as components of multiple new commercial products. The ASICs are typically large, high speed, algorithmically complex and implement novel functionality. The ASIC development process is driven by the commercial pressures of low cost and short schedules of multiple projects. It is carried out using a team of designers of varying experience including new staff. The dual emphasis o ...

Keywords: ASIC, application specific integrated circuits, concurrency, design, system, verification**3**[Reconfigurable computing: A methodology for FPGA to structured-ASIC synthesis](#)



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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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